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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/669,930	09/24/2003	Michael D. Gallant	03-0838 1496.00329	4636

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LSI LOGIC CORPORATION
1621 BARBER LANE
MS: D-106
MILPITAS, CA 95035

EXAMINER	
PHILIPPE, GIMS S	
ART UNIT	PAPER NUMBER
2621	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/27/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/669,930	GALLANT ET AL.	
	Examiner	Art Unit	
	Gims S. Philippe	2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 4/26/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This is a first office action in response to application no. 10/669,930 filed on September 24 2003 in which claims 1-20 are presented for examination.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-11, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Iwata (US Patent no. 6,198,771).

Regarding claims 1, 8, 11 and 20, Iwata discloses the same circuit, method and apparatus comprising a first circuit configured to generate a plurality of difference values by calculating an absolute difference between each pixel from a current block and a corresponding pixel from a reference block substantially simultaneously (See Iwata fig. 7, item 90-91, col. 9, lines 59-67, and col. 10, lines 1-4); a second circuit configured to generate a plurality of sum values by adding said difference values (See Iwata col. 10, lines 4-8); and a third circuit configured to generate at least one motion vector in response to said sum values (See Iwata col. 10, lines 8-13).

As per claim 2, most of the limitations of this claim have been noted in the above rejection of claim 1. In addition, Iwata further provides a first circuit comprising a plurality of processing elements each configured to generate one of the difference values (See Iwata fig. 7, processing elements 90-93 and col. 9, lines 59-64).

As per claim 3, most of the limitations of this claim have been noted in the above rejection of claim 1. In addition, Iwata further provides the processing elements logically configured as two-dimensional array receiving the pixels from the current block and the reference block on a first side of the array and presenting the difference values on a second side of the array (See Iwata col. 10, lines 47-52).

As per claim 4, most of the limitations of this claim have been noted in the above rejection of claim 1. In addition, Iwata further provides a second circuit comprising a plurality of adder circuits each configured to generate one of the sum values substantially simultaneously (See Iwata fig. 11, col. 14, lines 52-67, and col. 15, lines 1-9).

As per claim 5, most of the limitations of this claim have been noted in the above rejection of claim 4. In addition, Iwata further discloses the same circuit wherein each of the adder circuit comprises a plurality of stages connected in series, a first of the stages receive portion of the difference values and a last of the stages generates the one sum value (See Iwata fig. 11, and col. 14, lines 1-14).

As per claim 6-7 and 9, most of the limitations of these claims have been noted in the above rejection of claim 1. In addition, Iwata further discloses the same circuit wherein the third circuit comprises an adder circuit configured to generate a plurality of first intermediate values from said sum values; a storage circuit configured to generate a plurality of second intermediate values from said first intermediate values as said current block is moved through a search window; and a select circuit configured to generate said motion vector from said second intermediate values (See Iwata col. 4, lines 25-60).

As per claim 10, most of the limitations of this claim have been noted in the above rejection of claim 1. In addition, Iwata further discloses the same circuit wherein the first circuit comprises a plurality of processing elements each configured to generate one of said difference values, (ii) said second circuit comprises a plurality of first adder circuits each configured to generate one of said sum values and (iii) said third circuit comprises: a second adder circuit configured to generate a plurality of intermediate values from said sum values; a storage circuit configured to generate a plurality of second intermediate values from said intermediate values as said current block is moved through a search window; and a select circuit configured to generate said motion vector from said second intermediate values (See processing elements of fig. 7 to 10 and col. 10, lines 47-67 and col. 11, lines 1-34).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 12-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwata (US Patent no. 6198771).

As per claim 12-19, most of the limitations of these claims have been noted in the above rejection of claim 1.

It is noted that while Iwata does not specifically discloses the same claim language as noted in claims 12-19, however, the disclosure provided for figs. 11-14 and noted in col. 12 line 57 to col. 15, line 9 is considered either equivalent or renders the claimed limitations obvious to one skilled in the art at the time of the invention in order to derive motion vector while performing a full search block matching using an accumulated absolute value of the difference approach as noted by Iwata.

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Aoki et al. (US Patent no. 5793443) teaches motion vector detection circuit.

Aoki et al. (US Patent no. 5659364) teaches motion vector detection circuit.

Mizuno et al. (US Patent no. 6366616) teaches motion vector estimating apparatus with high speed and method of estimating motion vector.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gims S. Philippe whose telephone number is (571) 272-7336. The examiner can normally be reached on M-F (10:30-7:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dastouri Mehrdad can be reached on (571) 272-7418. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Gims S Philippe
Primary Examiner
Art Unit 2621

GSP

March 23, 2007